V.S.B. ENGINEERING COLLEGE, KARUR

Department of Electronics and Communication Engineering

Academic Year: 2018 - 2019 (EVEN Semester)

ASSIGNMENT QUESTIONS

Class: III Year / VI Semester B.E., ECE 'A','B,&'C' Sections

Name of Subject: Principles of Management

Sl. No.	Topics
1	Competitive intelligence
2	Consumer loyalty
3	Consumer risk
4	Copycat products
5	Corporate crimes
6	Corporate culture
7	Corporate social responsibility
8	Customer competency
9	Data security
10	Downtown revitalization
11	Employee coaching
12	Franchises
13	Green products
14	Intellectual capital
15	Job sculpting
16	Marketing ethics
17	Mergers
18	Outsourcing
19	Regional planning
20	Risk Management
21	Service initiatives
22	Strategic planning
23	Strikes
24	Tele Marketing
25	Underage workers
26	Unions
27	Whistle Blowing
28	Work ethic
29	Work life Balance
30	Work place diversity
31	Bias in promotion
32	Core competencies
33	Dress code
34	Employee benefit planning

Sl. No.	Topics
35	Employment Quality
36	Flexible scheduling
37	Human resources
38	Knowledge Management
39	Labor dispute
40	Mentoring
41	Public union
42	Reverse performance evaluation
43	Strategic Human resource management
44	Successive management
45	Team leadership
46	Telecommuting
47	Total quality management
48	Troubled employees
49	Workplace atmosphere
50	Workplace violence
51	Foreign exchange
52	Great recession
53	Green economy
54	Informal economy
55	Interest Rates
56	Minimum wages
57	National debt
58	Prevailing wages law

Signature of the Faculty Member **HOD**

V.S.B. ENGINEERING COLLEGE, KARUR

Department of Electronics and Communication Engineering

Academic Year: 2018-2019 (EVEN Semester

Assignment Questions

Class: III Year / VI Semester & ECE A,B 'C' Section

Name of Subject:CS6303-COMPUTER ARCHITECTURE

Name of Faculty member: Ms.S.Meena&Mr.M.Thanagavel

Sl. No.	Assignment Questions
1	What is the disadvantage of Ripple carry addition and how it is overcome in carry look ahead adder and draw the logic circuit CLA.
2	Design and explain a parallel priority interrupt hardware for a system with eight interrupt sources.
3	Explain Booth's Algorithm for the multiplication of signed two's complement numbers.
4	Discuss in detail about division algorithm in detail with diagram and examples.
5	Why is branch prediction algorithm needed?Differentiate between the static and dynamic techniques.
6	Assume the miss rate of an instruction cache is 2% and the miss rate of the data cache is 4%.If a processor has a CPI of 2 without any memory stalls and the miss penality is 100 cylces for all misses,determine how much faster a processor would run with a perfect cache that never missed.Assume the frequency of all loads and stores is 36%.
7	Discuss Shared memory multiprocessor with a neat diagram.
8	A pipelined processor uses delayed branch technique.Recommend any one of the following possibility for the design of the processor.In the first possiblilty,the processor has a 4-stage pipeline and two delay slot.In the second possibility,it has a 6-stage pipeline and two delay slots.Comparethe performanceof these two alternatives,taking only the branch penalty into account.Assume that 20% of the instructions are branch instructions and that delay slot.For the second alternative,the compiler is able to fill the second slot 25% of the time.
9	Discuss about the various techniques to represent instructions in a computer system.
10	Discuss about SISD,MIMD.

Sl. No.	Assignment Questions
11	Explain in detail about SPMD and VECTOR systems.
12	Describe SMT with an example.(Simultaneous Multithreading)

13	Translate the following C code to MIPS assembly code.Use a minimum number ofinstructions.Assume that I and k correspond to registers $s3 and $S5 and the base of the array save in $s6.What is the MIPS assembly code corresponding to this C segment?
	While(save[i]==k)
	i+1=1;

14	Add the numbers $(0.5)_{10}$ and $(0.4375)_{10}$ using the floating point addition. Multiply the numbers$(0.5)_{10}$ and$(0.4375)_{10}$ using the floating point multiplication.
15	Explain in detail about Superscalar processors.
16	Describe ARM-based Multicore processors.
17	Explain in detail about MIPS Instruction set and its applications.
18	Describe High Speed Memory Technology for cache.
19	Discuss Flash memory.
20	Explain the Differences between CISC & RISC
21	Explain the various generations of Computer.
22	Explain the Non –restoring division technique
23	Write in detail about Micro program control unit.
24	Explain the different wired controllers.
25	Explain with a diagram the design of a fast multiplier using carry save adder circuit
26	Describe in detail about associative memory.
27	Suppose you want to achieve a speed-up of 90 times faster with 100processors.What percentage of the original computation can be sequential?
28	Comparing paging and segmentation mechanisms for implementing the virtual memory.
29	Describe in detail about IOP organization.
30	Write short notes on the following (a) Magnetic disk drive (b) Optical drives

Sl. No.	Assignment Questions
31	Measure the performance of the computers: If computer A runs a program in 10 seconds, and computer B runs the same program in 15 seconds, how much faster is A over B? Formulate the equation of CPU execution time for a program.
32	Point out the impact on dynamic power: Suppose we develop a new simpler processor that has 85% of the capacitative load of the more complex older processor. Further assume that it has adjustable voltage ao that it can reduce voltage 5% compressed to processor B, which results in a 15% compressed to processor B, which results in a 15% shrink in frequency
33	Analyse Programmed I/O (ii)point out the Instructions executed by IOP.
34	Compare and contrast fine-grained multithreading. Coarse-grained multi-threading and simultaneous multi-threading.
35	Analyze the given problem: A byte addressable computer has a small data cache capable of holding eight 32-bit words. Each cache block contains 132-bit word. When a given program is executed, the processor reads data from the following sequence of hex addresses – 200, 204, 208, 20C, 2F4, 2F0,200,204,218, 21C, 24C, 2F4. The pattern is repeated four times.Assuming that the cache is initially empty, show the contents of the cache at the end of each pass, and compute the hit rate for a direct mapped cache.
36	Explain mapping function in cache memory to determine how memory blocks are placed incache.
37	Explain in detail about the Bus Arbitration techniques in DMA.
38	Describe the technologies for Building Processors and Memory. Differentiate uni-processors and multi-processors
39	Tabulate the IEEE 754 binary representation of the number - 0.75 10 i) single precision ii) double precision
40	Arrange in single precision IEEE 754 representation. i) 32.75 ii)18.125
41	(i).Show the Loop unrolling for multiple issue pipelines. ii). Illustrate the Concept of speculation and its difficulty
42	Suppose you want to perform two sums:one is a sum of 10 scalar variables and one is a matrix sum of a pair of two-dimensional arrays,with dimensions 10 by 10.For now let's assume only the matrix sum is parallelizable;We'll see soon how to parallelize scalar sums.What speed-up do you get with 10 versus 40 processors?.Next calculate the speed-ups assuming the matrices grow to 20 by 20.
43	(i)Give ALU control with suitable truth table. (ii)Differentiate R type instruction and memory instruction.

Sl. No.	Assignment Questions
44	Solve : Assume a program requires the execution of 50 × 106 FP istructions,110 × 106 INT instructions, 80 × 106 L/S instructions, and 16 × 106 branch instructions The CPI for each type of instruction is 1, 1, 4, and 2, respectively. Assume that the processor has a 2 GHz clock rate a) By how much must we improve the CPI of FP instructions if we want the program to run two times faster? b) By how much must we improve the CPI of L/S instructions c) if we want the program to run two times faster? d) By how much is the execution time of the program improved if the CPI of INT and FP Instructions are reduced by 40% and the CPI of L/S and Branch is reduced by 30%?
45	i) Explain static multiple issue processors. (8) ii)Infer what you understand from dynamic multiple issue processor?
46	Show with a suitable set of sequence of instructions what happens when the branch is taken,assuming the pipeline is optimized for branches that are not taken and that we moved the branch execution to the ID stage.
47	Analyze the multiplication of signed 2's complement numbers with algorithm and example.
48	Arrange the given number 0.0625 i) in single precision and ii) double precision formats
49	Calculate which code sequence will execute faster according to execution time for the following conditions: The c The computer with three instruction classes and CPI measurements as given below and instruction counts for each instruction class for the same program from two different compilers are given. Assume that the computer's clock rate is 1GHZ. Code from CPI for the instruction class A B C CPI 1 2 3 Code from CPI for the instruction class A B C Compiler1 2 1 2 Compiler2 2 1 1
50	Consider three different processors P1,P2 and P3 executing the same instruction set. P1 has 4GHz clock rate and CPI of 1.5. P2 has 2.5GHz clock rate and CPI f 1. P3 has 4GHz clock rate and has CPI of 2.2. (a) Which Processor has highest performance expressed in instruction per second? (b) If the processors each execute a program in 10seconds, find the number of cycles and number of instructions. (c) Reducing the execution time by 30% leads to increase in 20% of the CPI. What is the clock rate needed to get this reduction?
51	Examine the following sequence of instructions and identify the addressing modes used and the operation done in every instruction (1) Move (R5)+, R0 (2) Add(R5)+, R0 (3) Move R0, (R5) (4) Move 16(R5),R3 (5) Add #40, R5
52	Perform X+Y and Y-X using 2's complement for given the two binary numbers X=0000 1011

Sl. No.	Assignment Questions
	1110 1111 signed 2's complement numbers using the Booth algorithm. A=001110 AND b=111001 where A is multiplicand and B is multiplier.
53	Add the numbers$(0.75)_{10}$ and $(-0.275)_{10}$ in binary using the Floating point addition algorithm.
54	The following sequence of instructions are executed in the basic 5-stage pipelined processor: or r1,r2,r3 or r2,r1,r4 or r1,r1,r2 a)Indicate dependencies nad their type. b)Assume there is no forwarding in this pipelined processor.Indicate hazards and add NOP instructions to eliminate them. c)Assume there is full forwarding.Indicate hazards and add NOP instructions to eliminate them.
55	Formulate the performance equation of CPU (ii)Compose the factors that affect performance
56	Develop an algorithm to implement A*B. Assume A and B for a pair of signed 2's complement numbers with values : A = 010111, B = 101100.
57	Solve using Floating point multiplication algorithm i)1.10 10X 1010 and 9.200X10-5 ii)0.5 10 X 0.4375 10

V.S.B. ENGINEERING COLLEGE, KARUR
Department of Electronics and Communication Engineering
Assignment Questions

Subject Name: Computer Networks
Subject Handler: C.Moorthy &P.Deepiha **Class- III ECE-A B & C Section**

S.No	Questions
1.	Location-aware energy efficient virtual network embedding in software-defined optical data center networks
2.	Implementing flipped classroom and gamification teaching methods into computernetworks subject, by using cisco networking academy
3.	SDN enabled restoration with triggered precomputation in elastic optical inter-datacenter networks
4.	Education based new computer network simulator design and implementation
5.	Mobile network computer can better describe the future of information society
6.	Computer Network Security and Defense Technology Research
7.	A SDN-based deployment framework for Computer Network Defense Policy
8.	Proactive backup scheme of routes in distributed computer networks
9.	Analysis and comparative study of methods of improving the quick-speed of communication of multimedia data in computer networks
10.	Virtual network mapping for multicast services with max-min fairness of reliability
11.	Improved multipath adaptive routing model in computer networks with load balancing
12.	Computer network design of a company — A simplistic way
13.	Centralized monitoring of computer networks using Zenoss open source platform
14.	Fast rerouting algorithm in distributed computer networks based on subnet routing method
15.	Analysis of co-authorship in computer networks using centrality measures
16.	Study on Applying the Neural Network in Computer Network Security Assessment
17.	Multimedia teaching and learning for computer networks subject in the direct problem-based learning approach: A pilot study
18.	Analysis of techniques for isolation of faults in survivable computer networks
19.	Packet Tracer Simulation Tool as Pedagogy to Enhance Learning of Computer NetworkConcepts
20.	Ad-hoc lab computer network configuration using remote resources
21.	A wearable computer wireless sensor network
22.	Automatic Detection of Computer Network Traffic Anomalies based on Eccentricity Analysis
23.	Leveraging mixed-strategy gaming to realize incentive-driven VNF service chain provisioning in broker-based elastic optical inter-datacenter networks
24.	Research on computer virus source modeling with immune characteristics
25.	ANSwer: Combining NFV and SDN features for network resilience strategies
26.	Network configuration with quality of service abstractions for SDN and legacy networks
27.	Markov model of normal conduct template of computer systems network objects
28.	Optimization of the computer network work based on adaptive management of node equipment
29.	Increase the speed of detection and recognition of computer attacks in combined diagonalized neural networks
30.	Software-Defined Networking: A Comprehensive Survey
31.	Unified Software-Defined Online Network Experiment Platform for Campus Education
32.	Computer network security evaluation based on intelligent algorithm
33.	Resource allocation in electrical/optical hybrid switching data center networks
34.	Computer vision approaches based on deep learning and neural networks: Deep neural networks for video analysis of human pose estimation
35.	IEEE Standard for Local and metropolitan area networks-- Bridges and

	Bridged Networks - Amendment 23: Application Virtual Local Area Network (VLAN) Type, Length, Value (TLV)
36.	Energy-optimal routing on VCSEL-based interconnected networks
37.	Deadline-aware and energy-efficient dynamic flow scheduling in data center network
38.	Dynamic model SIR of the spread of virus inside computers in scale free network
39.	Profiling IP hosts based on traffic behavior
40.	HyperFlex: Demonstrating control-plane isolation for virtual software-defined networks
41.	Resources management in virtualized Information Centric Wireless Network
42.	A threat risk estimation model for computer network security
43.	The ACTION project: Application coordinating with Transport, IP and optical networks
44.	IRS: Incentive Based Routing Strategy for Socially Aware Delay Tolerant Networks
45.	Topology based reliable virtual network embedding from a QoE perspective
46.	Adaptive modulation and flexible resource allocation in space-division- multiplexed elastic optical networks
47.	Performance analysis of software defined networks
48.	Two approaches to dynamic power management in energy-aware computer networks - methodological considerations
49.	Multi-level reliability architecture for network slicing in metro networks
50.	A research platform for software defined satellite networks
51.	FlowMap: Improving network management with SDN
52.	PODCA: a passive optical data center network architecture
53.	Energy efficiency versus reliability performance in optical backbone networks [invited]
54.	Real-Time Verification of Network Properties Using Atomic Predicates
55.	A network virtualization framework for information centric data center networks
56.	Control-plane slicing methods in multi-tenant software defined networks
57.	Classification of Computer Network Users with Convolutional Neural Networks
58.	Ethernet switch/terminal simulators for novices to learn computer networks
59.	Inter-domain optimization and orchestration for optical datacenter networks

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Department of Electronics and Communication Engineering

Academic Year: 2018 - 2019 (EVEN Semester)

ASSIGNMENT QUESTIONS

Class: III Year / VI Semester B.E., ECE'A, 'B'& 'C' Section
Name of Subject: VLSI Design
Name of Faculty member: Dr.M.Sundaram,S.Satish

Sl. No.	Topics
1	Ripple Carry Adder
2	Carry look ahead Adders
3	Booth Multiplier
4	Wallace Tree Multiplier
5	Array Multiplier
6	Serial Divider
7	Parallel Divider
8	Barrel Shifters
9	32 Bit Barrel Shifters
10	ALU
11	Multipliers
12	Parity generators
13	Comparators
14	Zero/One Detectors
15	Counters
16	SRAM
17	DRAM
18	ROM
19	Serial access memories
20	Gate array based ASIC
21	Field Programmable Gate Array
22	RAM Based FPGA Routing
23	Vertical Routing FPGA
24	Horizontal Routing FPGA
25	Xilinix FPGA
26	Programmable Logic Devices
27	Carry skip Adder
28	Manchester Carry Chain Adder
29	Carry Select Adder
30	Carry Increment Adder
31	Serial Multiplier
32	Parallel Multiplier
33	Master Slave Edge Triggered Register

Sl. No.	Topics
34	Pseudo Static Dynamic Latch
35	True Single Phase Clocked Register
36	CPLDs
37	Standard Cells
38	Programmable Array Logic
39	Parameter influencing low power design
40	CMOS Testing
41	Latch up problem
42	Logarithmic Shifter
43	Braun Multiplier
44	Baugh-Wooley Multiplier
45	Standard cell library
46	Channeled gate array
47	Channel less gate array
48	Structured gate array
49	FPGA building block architecture
50	NOR based ROM
51	NAND based ROM
52	Clocking stratergies
53	Timing issues in sequential logic circuit
54	Clocked CMOS Register
55	Techniques for reducing Dynamic Power
56	Techniques for reducing short circuit power
57	Techniques for reducing Leakage power
58	Design flow of ASIC

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Academic Year: 2018-2019 (EVEN Semester)

Assignment Questions

Class: III Year / VI Semester & ECE 'A', 'B' & 'C' Sections
Name of Subject: EC 6602 – Antenna and Wave Propagation
Name of Faculty member: Mr.R.R.Jegan &Ms.P.Deepiha

Sl. No.	Questions
1	An ultra-wideband horizontally polarized omnidirectional connected vivaldi array antenna
2	Design of a Low-Profile Dual-Polarized Stepped Slot Antenna Array for Base Station
3	A Broadband Low-Profile Circular-Polarized Antenna on an AMC Reflector
4	Uniplanar differentially driven ultrawideband polarization diversity antenna with band-notched characteristics
5	A Low-Profile Dual-Polarized Microstrip Antenna Array for Dual-Mode OAM Applications
6	Electrically small metamaterial-inspired tri-band antenna with meta-mode
7	A Frequency Diversity Printed-Yagi Antenna Element for Apertures Selectivity Wideband Array Application
8	Dense, planar arrays of compact Resonant Cavity Antenna
9	A planar multiband Antenna based on CRLH-TL ZOR for 4G compact mobile terminal applications
10	A dual-polarized dual-band antenna with omni-directional radiation patterns
11	Radiation Efficiency Improvement of a Balanced Miniature IFA-Inspired Circular Antenna
12	Dual band multi-beam base station Antennas
13	A Single Patch Antenna With Broadside and Conical Radiation Patterns for 3G/4G Pattern Diversity
14	Compact ultra wide band sinuous Antenna
15	A single radiator with four decoupled ports for four by four MIMO Antenna and systems
16	Antenna Array Design and System for Directional Networking
17	Combined-type dual-wideband and triple-wideband LTE Antenna for the tablet device
18	A Switchable-Frequency Slot-Ring Antenna Element for Designing a Reconfigurable Array
19	A Reconfigurable Dual-Polarization Slot-Ring Antenna Element With Wide Bandwidth for Array Applications
20	5G Antenna array with wide-angle beam steering and dual linear polarizations
21	A conformal UHF Antenna for cargo helicopter belly
22	A Multifeed Antenna for High-Efficiency On- Antenna Power Combining
23	Frequency-Reconfigurable Bow-Tie Antenna for Bluetooth, wimax, and WLAN Applications
24	Miniaturized omnidirectional horizontally polarized antenna
25	A high-gain dielectric resonator Antenna array fed by back-cavity
26	Dual band, dual polarized, rail mount MIMO stadium Antenna
27	Design of Multiple-Polarization Transmitarray Antenna Using Rectangle Ring Slot Elements
28	Compact Offset Microstrip-Fed MIMO Antenna for Band-Notched UWB Applications
29	A K-band series-fed microstip array Antenna with low sidelobe for anticollision radar application
30	Low-profile, quasi-omnidirectional substrate integrated waveguide (siw) multihorn antenna
31	LHCP and RHCP Substrate Integrated Waveguide Antenna Arrays for Millimeter-Wave Applications

Sl. No.	Questions
32	Low-RCS Monopolar Patch Antenna Based on a Dual-Ring Metamaterial Absorber
33	Low-RCS, High-Gain, and Wideband Mushroom Antenna
34	Planar circularly polarized endfire Antenna based on superposition of complementary dipoles
35	SIW-integrated patch Antenna backed air-filled cavity for 5G MMW appilcations
36	Dual-Band Slot Helix Antenna for Global Positioning Satellite Applications
37	MIMO monopole microstrip Antenna for LTE
38	Broadband Dual-Polarized Omnidirectional Antenna for 2G/3G/LTE/wifi Applications
39	Very-Low-Profile, Triband, Two- Antenna System for WLAN Notebook Computers
40	Quad-band microstrip Antenna with only one slot on the edge
41	Design of a Broadband Polarization-Reconfigurable Fabry–Perot Resonator Antenna
42	Gain Enhancement of a Broadband Symmetrical Dual-Loop Antenna Using Shorting Pins
43	Integration of very-low-profile slot Antenna into notebook metal cover with narrow bezel
44	SIW series-fed patch Antenna array based on transverse slot excitation for millimeter wave (MMW) applications
45	A wideband horizontally polarized omnidirectional Antenna using tightly coupled array mechanism
46	Metamaterial-based wideband shorting-wall loaded mushroom array Antenna
47	Wideband Circularly Polarized Antenna With Stair-Shaped Dielectric Resonator and Open-Ended Slot Ground
48	Single-anchor indoor localization using espar antenna
49	Analysis and Design of a Broadband Multifeed Tightly Coupled Patch Array Antenna
50	Dual-band microstrip Antenna fed by coaxial probe
51	Dual-band microstrip circular patch antenna with monopolar radiation pattern
52	Optimization of Log-Periodic Dipole Array Antenna for Wideband Omnidirectional Radiation
53	A Broadband Horizontally Polarized Omnidirectional Antenna for VHF Application
54	Low Side-Lobe Substrate-Integrated-Waveguide Antenna Array Using Broadband Unequal Feeding Network for Millimeter-Wave Handset Device

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Signature of the faculty with date: **HOD**

V.S.B Engineering College, Karur

Department of Electronics and Communication Engineering

MEDICAL ELCTRONIVS

IIIrd Year ECE'A','B'& 'C'

ASSIGNMENT QUESTIONS

S.No	Assignment Topics
1	Blood gas analyzer
2	Medical glucose Monitor
3	Infrared and Digital Thermometers
4	Defibrillator for medical electronics
5	Sphygmomanometer
6	MRI for medical electronics
7	Fetal Monitor
8	CPAP Machine
9	Pulse Oximeter
10	Infusion pump
11	Hearing aid
12	Personal activity monitor
13	Anesthesia Machine
14	Drug Dispenser
15	Neuro Stimulator
16	Nerve stimulator
17	Otoscope/Ophthalmoscope
18	X-Ray Mobile
19	Ultrasound (3 probes)
20	Gastroscope (With halogen light source)
21	Colonoscope (With halogen light source)
22	Electrosurgical Unit (Monopolar-bipolar)
23	Pulsoximeter
24	Incubator neonate

25 Duodenoscope
26 Fiber bronchoscope
27 Holter Monitor and Analyser
28 Phototherapy
29 Bone Densitometry machine
30 Ultra-sonography machine
31 Mammography Machine
32 Computarized 32-channel Electroenchephalograph
33 Neuro Electrophysiology
34 Retinal Camera
35 Perimetry Machine
36 Tonometry machine
37 Embryo Cryo-Preservation
38 Electronic Muscle Stimulator
39 Paraffin Wax Bath
40 Horizontal Steam Sterilizer
41 EtOSterilizer
42 Cystoscope
43 Digital Subtraction Angiography
44 Laryngoscope
45 Cyber Medicine
46 Palm Vein Technology
47 Dual Energy X-ray Absorptiometry
48 Palm Vein Technology
49 Artificial blood: polymerized human hemoglobin
50 3D Obstetric Ultra sound Imaging
51 Brain Implants
52 Disease Detection Using Bio-robotics
53 Virtual Surgery
54 Frequency modulation for skin permeability
55 Medical Mirror
56 Eye Directive Wheelchair